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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,700	12/07/2001	Hong-Sik Jeong	5649-905	5150

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EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,700	JEONG ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-25 and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 6-25 and 27-29 have been considered but are moot in view of the new ground(s) of rejection.

The indicated allowability of claims 6-24 and 26-27 is withdrawn in view of the newly discovered reference(s) to Habu et al. (U.S. 6,078,073) Dennison (U.S. 5,401,681). Rejections based on the newly cited reference(s) follow.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 6, 8, 10, 12-13, 15, 17-19, 21 and 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Habu et al. (U.S. 6,078,073).

Habu discloses a gate electrode structure with

(6); (15); (25) forming a pattern comprising a pair of mesa regions (2) on a substrate (100) (see Figure 7A);

forming a first insulating layer (3) on the pair of mesa regions (2) (see Figure 7A);

forming a second insulating layer (4) on the pair of mesa regions (2) and the substrate (100) (see Figure 7A);

forming a capping layer (7) on the second insulating layer (4) (see Figure 7B);

patterning the capping layer (7) and the second insulating layer (4) (see Figure 7C);

forming insulating spacers (6') on sidewalls of the second insulating layer (4) such that the second insulating layer (4) is enclosed by the insulating spacers (6'), the capping layer (7), the first insulating layer (3), and the substrate (100) (see Figure 7D);

(8); (19) further comprising: applying a cleaning solution to the integrated circuit device so as to expose a contact region between the pair of mesa regions by removing at least a portion of a native oxide layer from the contact region (see Figure 15F);

(10); (21) further comprising: forming a conductive layer on the pair of mesa regions and the substrate so as to fill a contact region between the pair of mesa regions and to cover the mesa regions; removing a portion of the conductive layer such that an

upper surface of the first insulating layer, opposite the substrate, is exposed (see Figure 15F);

(12); (24) wherein the capping layer may comprise at least one of silicon oxide, silicon nitride, undoped polysilicon, doped polysilicon, or Al_2O_3 (see column 9, lines 20-25);

(13) wherein forming the insulating spacers comprises: forming a third insulating layer on the capping layer, the sidewalls of the second insulating layer, and the substrate; etching the third insulating layer so as to remove at least a portion of the third insulating layer from the substrate and an upper surface of the capping layer, opposite the substrate (see Figure 6E);

(17) wherein forming the insulating spacers comprise: forming a third insulating layer on the capping layer, the sidewalls of the second insulating layer, and the etch stop layer; etching the third insulating layer so as to remove at least a portion of the third insulating layer from the second insulating layer and an upper surface of the capping layer, opposite the substrate (see Figure 6E);

(18) further comprising: removing at least a portion of the etch stop layer from a contact region between the pair of mesa regions (see Figure 7C).

Claims 7, 16 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Habu et al. (U.S. 6,078,073) in view of Jones et al. (U.S. 5,549,786).

Habu teaches the above outlined features except for wherein the second insulating layer is a spin on glass layer. However, Jones discloses an SOG plasma

etch process with **(7); (16); (28); (29)** wherein the second insulating layer is a spin on glass layer (see column 6, lines 50-60). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the above teachings of Habu and Jones by forming a gate electrode or an interconnection is interchangeable. The conductive layer is patterned to form whether an interconnection or a gate electrode to meet its end use during manufacturing a semiconductor device.

Claims 14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Habu et al. (U.S. 6,078,073).

Habu discloses the claimed invention except for wherein each of the insulating spacers has a width in a range of about 50Å to about 200Å. It would have been obvious to one of that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 and In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

When the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing unexpected results or the criticality of the claimed range. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims 14 and 23. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves

unexpected results relative to the prior art range." In re Woodruff , 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP ' 716.02 - ' 716.02(g) for a discussion of criticality and unexpected results.

Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Habu et al. (U.S. 6,078,073).

Habu discloses the claimed invention except for wherein the cleaning solution comprises at least one of hydrofluoric (HF) acid or a mixture of NH_4OH, H_2O_2, and H_2O. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the specific cleaning solution that is suitable for its objectinve, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Habu et al. (U.S. 6,078,073) in view of Dennison (U.S. 5,401,681).

Habu teaches everything above except for wherein removing the portion of the conductive layer comprises: chemical mechanical polishing the conductive layer such that the upper surface of the first insulating layer, opposite the substrate, is exposed. However, Dennison discloses a semiconductor device with **(11); (22)** wherein removing the portion of the conductive layer comprises: chemical mechanical polishing the conductive layer such that the upper surface of the first insulating layer, opposite the

substrate, is exposed (see column 6, lines 55-60). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to combine the above teachings of Habu and Dennison by applying chemical mechanical polishing process to remove a conductive material. The conductive layer is patterned to form whether an interconnection or a gate electrode to meet its end use during manufacturing a semiconductor device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CAL
July 9, 2004

CANDIDA EVERHART
PRIMARY EXAMINER